DATA SHEET

TDA4650
Multistandard colour decoder, with negative colour difference output signals

Preliminary specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

Multistandard colour decoder, with negative colour difference output signals

TDA4650

FEATURES

Identifies and demodulates PAL, SECAM, NTSC 3.58 and NTSC 4.43 chrominance signals with:

- Identification
  - automatic standard identification by sequential inquiry
  - secure SECAM identification at 50 Hz only, with PAL priority
  - four switched outputs for chrominance filter selection and display control
  - external service switch for oscillator adjustment
- PAL / NTSC demodulation
  - H (burst) and V blanking
  - PAL switch (disabled for NTSC)
  - NTSC phase shift (disabled for PAL)
  - PLL-controlled reference oscillator
  - two reference oscillator crystals on separate pins with automatic switching
  - quadrature demodulator with subcarrier reference
- SECAM demodulation
  - limiter-amplifier
  - quadrature-demodulator with a single external reference tuned circuit
  - alternate line blanking, H and V blanking
  - de-emphasis
- Gain controlled chrominance amplifier
- ACC demodulation controlled by system scanning
- Internal colour-difference signal output filters to remove the residual subcarrier

GENERAL DESCRIPTION

The TDA4650 is a monolitic integrated multistandard colour decoder for PAL, SECAM and NTSC (3.58 and 4.43 MHz) with negative colour difference output signals. The colour-difference output signals are fed to the TDA4660/TDA4661, Switched capacitor delay line.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_p	supply voltage range (pin 13)		10.8	12.0	13.2	V
I_p	supply current (pin 13)		–	60	–	mA
$v_{i(p-p)}$	chrominance input voltage (pin 15) (peak-to-peak value)		20	100	400	mV
$V_{o(p-p)}$	colour-difference output voltage (pin 1) (peak-to-peak value)	PAL/NTSC	0.42	0.525	0.66	V
	colour-difference output voltage (pin 3) (peak-to-peak value)	PAL/NTSC	0.53	0.665	0.84	V
	colour-difference output voltage (pin 1) (peak-to-peak value)	SECAM	0.83	1.05	1.32	V
	colour-difference output voltage (pin 3) (peak-to-peak value)	SECAM	1.06	1.33	1.67	V

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4650	28	DIL	plastic	SOT117[(1)]
TDA4650WP	28	PLCC	plastic	SOT261[(2)]

Note

1. SOT117-1; 1996 November 28.
2. SOT261-2; 1996 November 28.

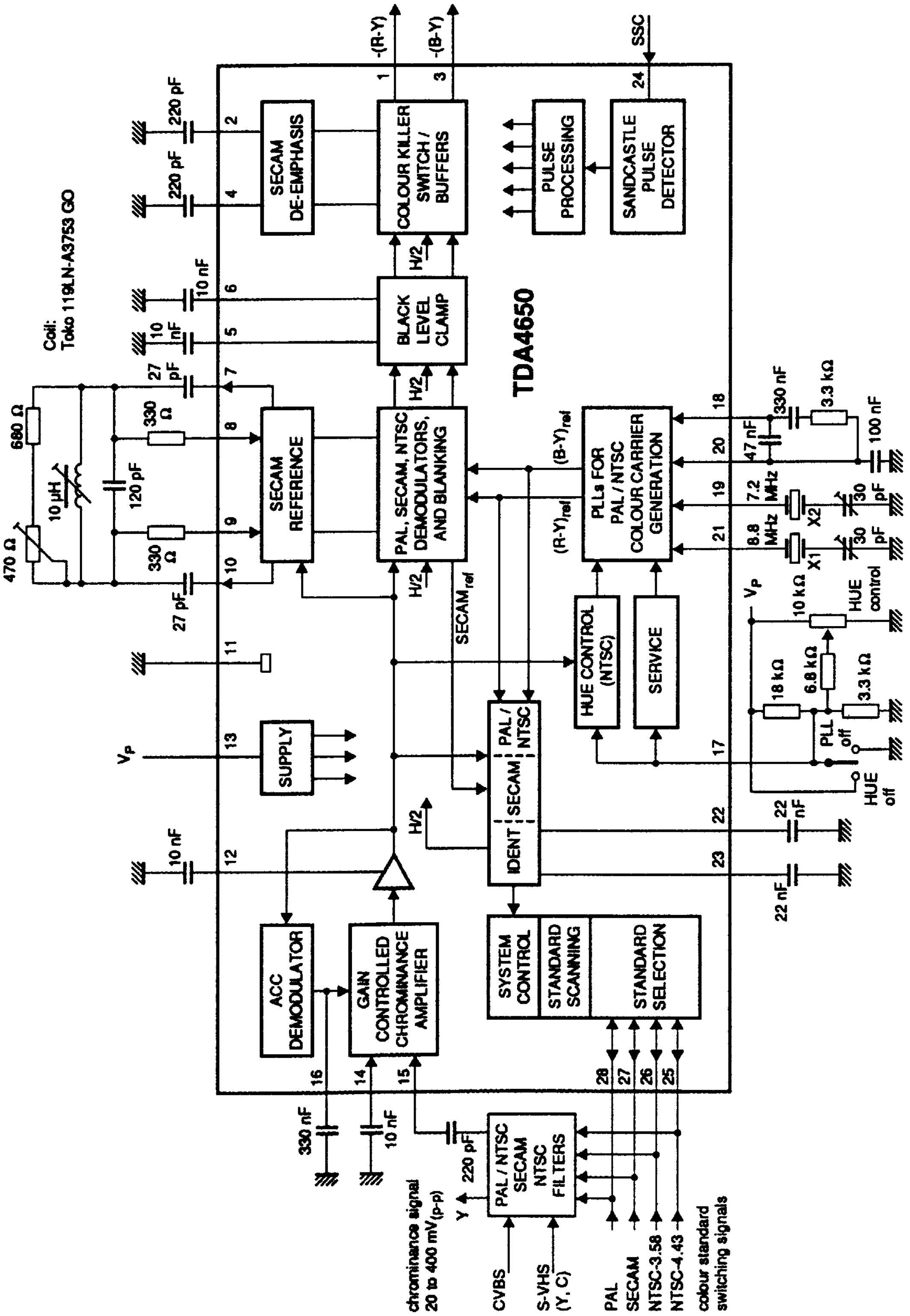


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$-(R\text{-}Y)_o$	1	–(R-Y) output
$-(R\text{-}Y)_{DE}$	2	(R-Y) de-emphasis
$-(B\text{-}Y)_o$	3	–(B-Y) output
$-(B\text{-}Y)_{DE}$	4	(B-Y) de-emphasis
$-(B\text{-}Y)_{CL}$	5	(B-Y) clamping
$-(R\text{-}Y)_{CL}$	6	(R-Y) clamping
SEC_{REF}	7	SECAM reference tuned circuit
SEC_{REF}	8	SECAM reference tuned circuit
SEC_{REF}	9	SECAM reference tuned circuit
SEC_{REF}	10	SECAM reference tuned circuit
GND	11	ground
C_D	12	DC for demodulators
V_P	13	supply voltage
C_{DC}	14	DC feedback

SYMBOL	PIN	DESCRIPTION
CHR_I	15	chrominance input
C_{ACC}	16	automatic colour control
HUE	17	hue control
PLL	18	PLL time constant
OSC1	19	input for 7.15 MHz oscillator
C_{PLL}	20	PLL DC reference
OSC2	21	input for 8.86 MHz oscillator
N_{IDENT}	22	NTSC identification
P_{IDENT}	23	PAL/SECAM identification
SSC	24	super sandcastle pulse input
N_{O1}	25	NTSC (4.43 MHz) identification
N_{O2}	26	NTSC (3.58 MHz) identification
SEC_o	27	SECAM identification
PAL_o	28	PAL identification

PIN CONFIGURATIONS

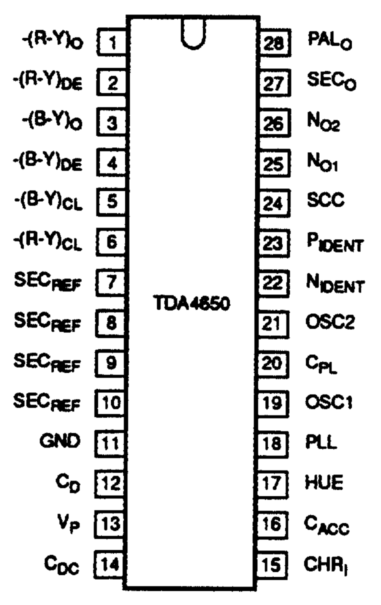


Fig.2 Pin configuration for DIL package

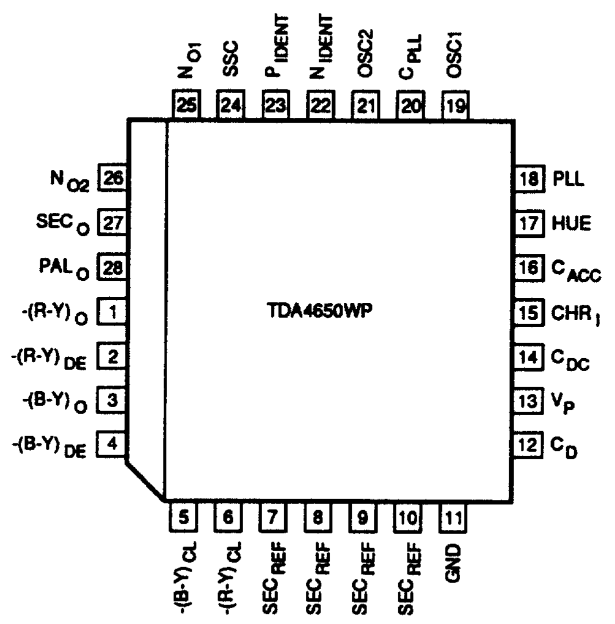


Fig.3 Pin configuration for PLCC package.

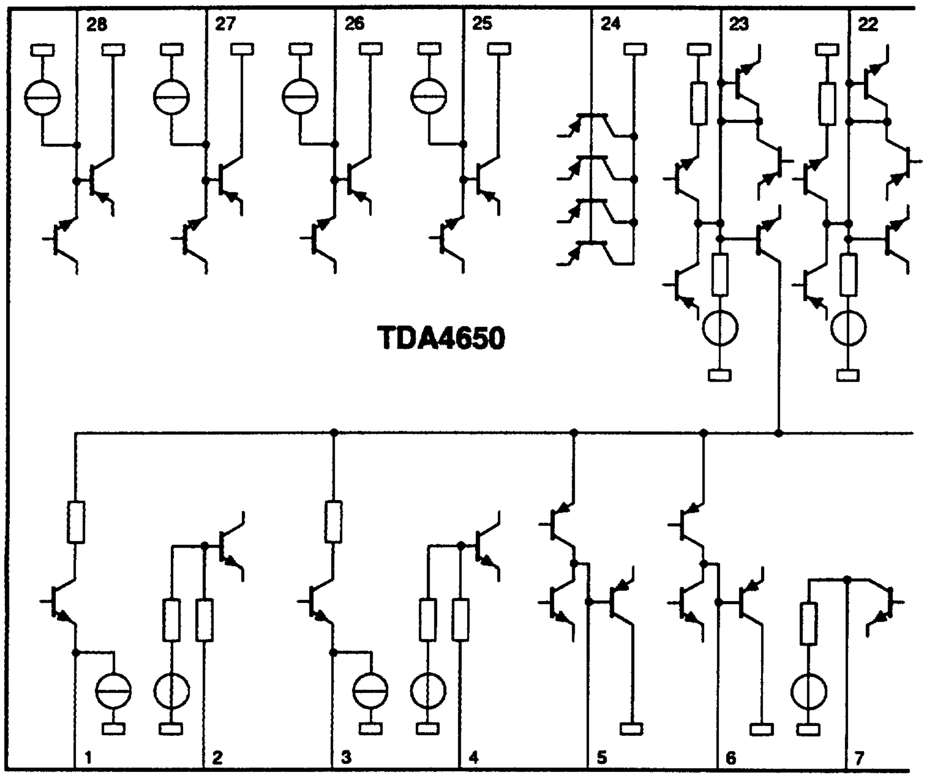


Fig.4 Internal circuits (continued in Fig.5)

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 13) –	13.2	V	
V_I	voltage range at pins 1, 3, 17 and 24 to 28	0	V_P	V
I_o	output current (pins 1 and 3)	–	–5	mA
$I_{i/o}$	input/output current (pins 25 to 28)	–	–5	µA
T_{stg}	storage temperature range	–25	+ 150	°C
T_{amb}	operating ambient temperature range	0	+ 70	°C
$R_{th\ j\text{-}a}$	from junction to ambient in free air:			
	SOT117	–	37	K/W
	SOT261	–	70	K/W
P_{tot}	total power dissipation (SOT117)	–	1.4	W
	total power dissipation (SOT261)	–	1.1	W

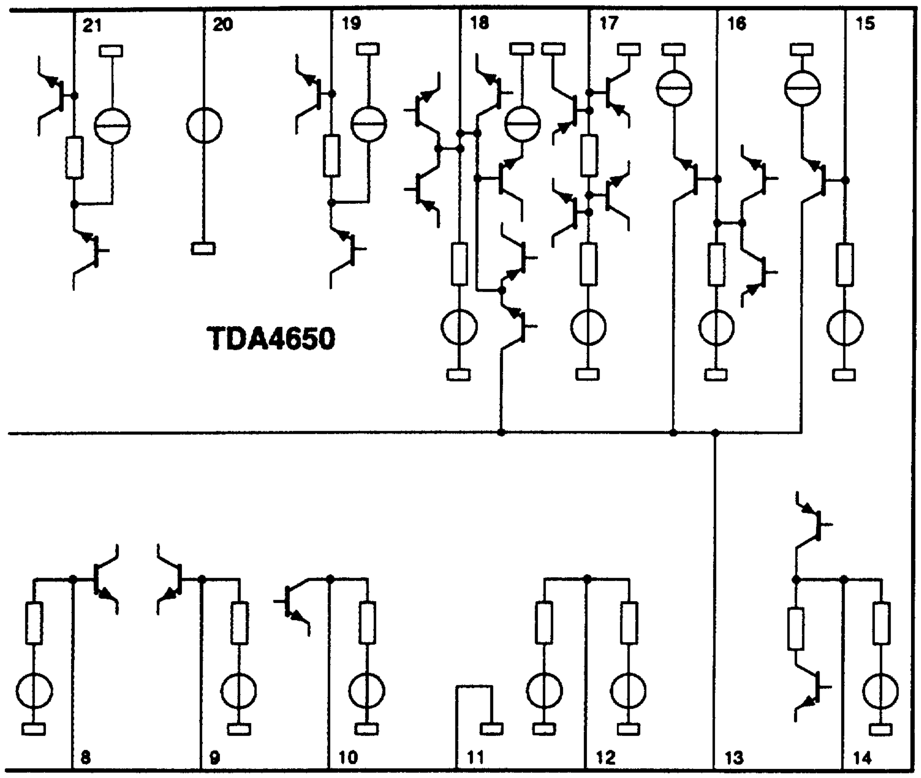


Fig.5 Internal circuits (continued from Fig.4)

CHARACTERISTICS

All voltages are measured to GND (pin 11); V_P = 12 V; chrominance input signal $V_{15(p-p)}$ = 100 mV (with 75 % colour bar signal); 4 µs burst-blanking pulse and vertical blanking superimposed on super sandcastle pulse; T_{amb} = 25 °C; measured in test circuit of Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage range		10.8	12.0	13.2	V
I_P	supply current		50	60	80	mA
Chrominance part						
$V_{i(p-p)}$	input signal (pin 15) (peak-to-peak value)		20	100	400	mV
R_i	input resistance (pin 15)		7	10	13	kΩ
C_i	input capacitance (pin 15)		–	4	5	pF
Demodulator part (PAL/NTSC)						
$V_{1(p-p)}$	colour difference –(R–Y) output signal (peak-to-peak value)	at nominal phase of hue control	0.42	0.525	0.66	V
$V_{3(p-p)}$	colour difference –(B–Y) output signal (peak-to-peak value)	at nominal phase of hue control	0.53	0.665	0.84	V
V_1/V_3	ratio of colour difference signals (R–Y)/(B–Y) for NTSC	at nominal phase of hue control	0.75	0.79	0.83	
V_1/V_1	ratio of PAL/NTSC signals $(R–Y)_{PAL}/(R–Y)_{NTSC}$	at nominal phase of hue control	–	–	1	dB
m	signal linearity	$V_{1(p-p)}$ = 0.8 V – (R–Y)	0.8	–	–	
		$V_{3(p-p)}$ = 1.0 V – (B–Y)	0.8	–	–	
$V_{1,3}$	DC output level	proportional to V_P	6.3	6.8	7.3	V
	H/2 ripple at CD outputs	without colour bars	–	–	10	mV
$V_{1,3(p-p)}$	residual carrier at CD outputs (peak-to-peak value)	4.43 MHz	–	–	10	mV
		8.87 MHz	–	–	30	mV
$Z_{1,3}$	output impedance		–	–	200	Ω
Demodulator part (SECAM); note 1						
$V_{1(p-p)}$	colour difference –(R–Y) output signal (peak-to-peak value)	every second line blanked	0.83	1.05	1.32	V
$V_{3(p-p)}$	colour difference –(B–Y) output signal (peak-to-peak value)	every second line blanked	1.06	1.33	1.67	V
$V_{1,3}$	DC output level	proportional to V_P	6.3	6.8	7.3	V
	H/2 ripple at CD outputs	without colour bars every second line blanked	–	–	10	mV
$V_{1,3(p–p)}$	residual carrier at CD outputs (peak-to-peak value)	4.43 MHz	–	–	30	mV
		8.87 MHz	–	–	30	mV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Demodulator part (SECAM) (continued); note 1						
$\Delta V_{1,3}/\Delta V_P$	shift of blanking levels relative to demodulated f_o levels		–	–	3	mV/V
$\Delta V_1/\Delta T$			–	0.16	–	mV/K
$\Delta V_3/\Delta T$			–	–0.25	–	mV/K
Hue control part						
ϕ	phase shift of reference carrier relative to phase at V_{17} = 3 V	V_{17} = 2 V	–30	–40	–	deg
	phase shift of reference carrier	V_{17} = 3 V	–	0	± 5	deg
	phase shift of reference carrier relative to phase at V_{17} = 3 V	V_{17} = 4 V	30	40	–	deg
V_{17}	internal bias voltage		–	3	–	V
	switching voltage for oscillator adjustment	burst OFF; colour ON	0	–	0.5	V
	switching voltage for forced colour ON	burst ON; colour ON	5.5	–	V_P	V
R_{17}	input resistance		3.8	5.0	6.2	kΩ
Reference oscillator (PLL); note 2						
$R_{19,21}$	input resistance		–	350	–	Ω
$C_{19,21}$	input resistance		–	–	10	pF
f_c	catching range	at 4.43 MHz	± 400	–	–	Hz
		at 3.57 MHz	± 330	–	–	Hz
Identification part switching voltages for chrominance filters and crystals: at pin 28 for PAL at pin 27 for SECAM at pin 26 for NTSC (3.58 MHz) at pin 25 for NTSC (4.43 MHz)						
$V_{28\ to\ 25}$	switching voltages	control voltage OFF state	–	0.05	0.5	V
		control voltage ON state; during scanning	2.35	2.45	2.55	V
		control voltage ON state; internal forced	5.6	5.8	6.0	V
		control voltage ON state; external forced	9.0	-	V_P	V
$I_{28\ to\ 25}$	output currents		–	–	–3	mA
t_d	delay time for system hold		2	–	3	cycles
	delay time for colour ON		2	–	3	cycles
	delay time for colour OFF		0	–	1	cycles
t_s	scanning time for each standard	note 3	–	4	–	cycles

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Super sandcastle pulse detector (note 4)						
V_{24}	input voltage pulse levels to separate V and H blanking pulses	pulse ON	1.3	1.6	1.9	V
		pulse OFF	1.1	1.4	1.7	V
	voltage pulse amplitude		2.0	2.5	3.0	V
	input voltage pulse levels to separate H blanking pulse	pulse ON	3.3	3.6	3.9	V
		pulse OFF	3.1	3.4	3.7	V
	voltage pulse amplitude		4.1	4.5	4.9	V
	input voltage pulse levels to separate burst gating pulse	pulse ON	6.2	6.6	7.0	V
		pulse OFF	6.0	6.4	6.8	V
	voltage pulse amplitude		7.7	–	V_P	V
	input voltage	during line scan	–	–	1.0	V
I_{24}	input current	during line scan	–	–	–100	μA

Notes to the characteristics

1. For the SECAM standard, amplitude and H/2 ripple content of the CD signals (R–Y) and (B–Y) depend on the characteristics of the external tuned circuit at pins 7 to 10. The resonant frequency of the external tuned circuit must be adjusted such that the demodulated f_o voltage level is zero in the –(B–Y) output channel at pin 3.
   Now it is possible to adjust the quality of the external circuit such that the demodulated f_o voltage level is zero in the –(R–Y) output channel at pin 1. If necessary, the f_o voltage level in the –(B–Y) output channel must be readjusted to zero by the coil of the tuned circuit.
   The external capacitors at the pins 2 and 4 (220 pF each) are matched to the internal resistances of the de-emphasis network such that every alternate scanned line is blanked.
2. The f_o frequencies of the 8.8 MHz crystal at pin 21, and the 7.2 MHz crystal at pin 19, can be adjusted when the voltage at pin 17 is less than 0.5 V (burst OFF), thus providing double subcarrier frequencies of the chrominance signal.
3. The inquiry sequence for the standard is: PAL – SECAM – NTSC (3.58 MHz) – NTSC (4.43 MHz).
   PAL has priority with respect to SECAM, etc.
4. The super sandcastle pulse is compared with three internal threshold levels which are proportional to V_P.

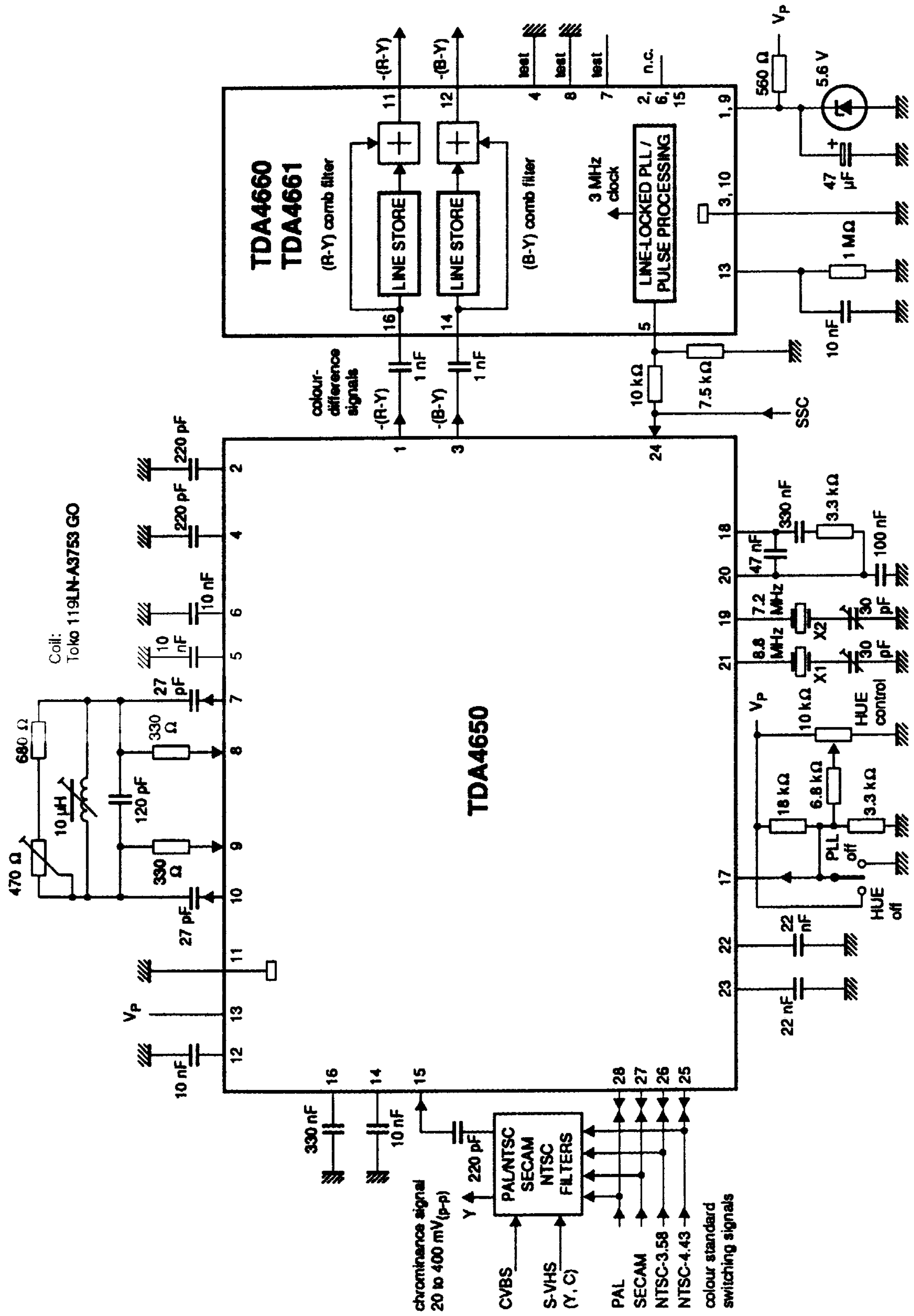
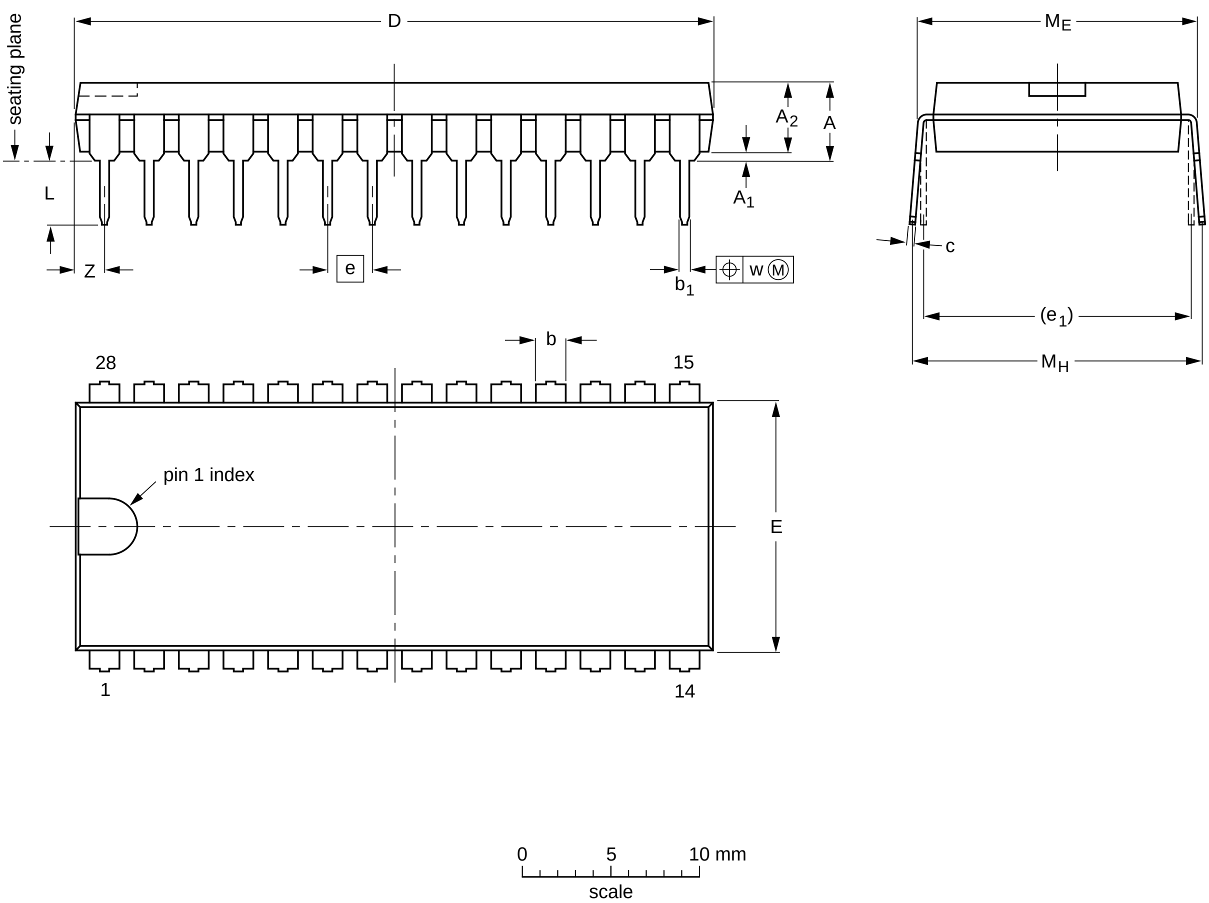


Fig.6 Application diagram with the switched capacitor delay line TDA4660/1.

PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil) SOT117-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

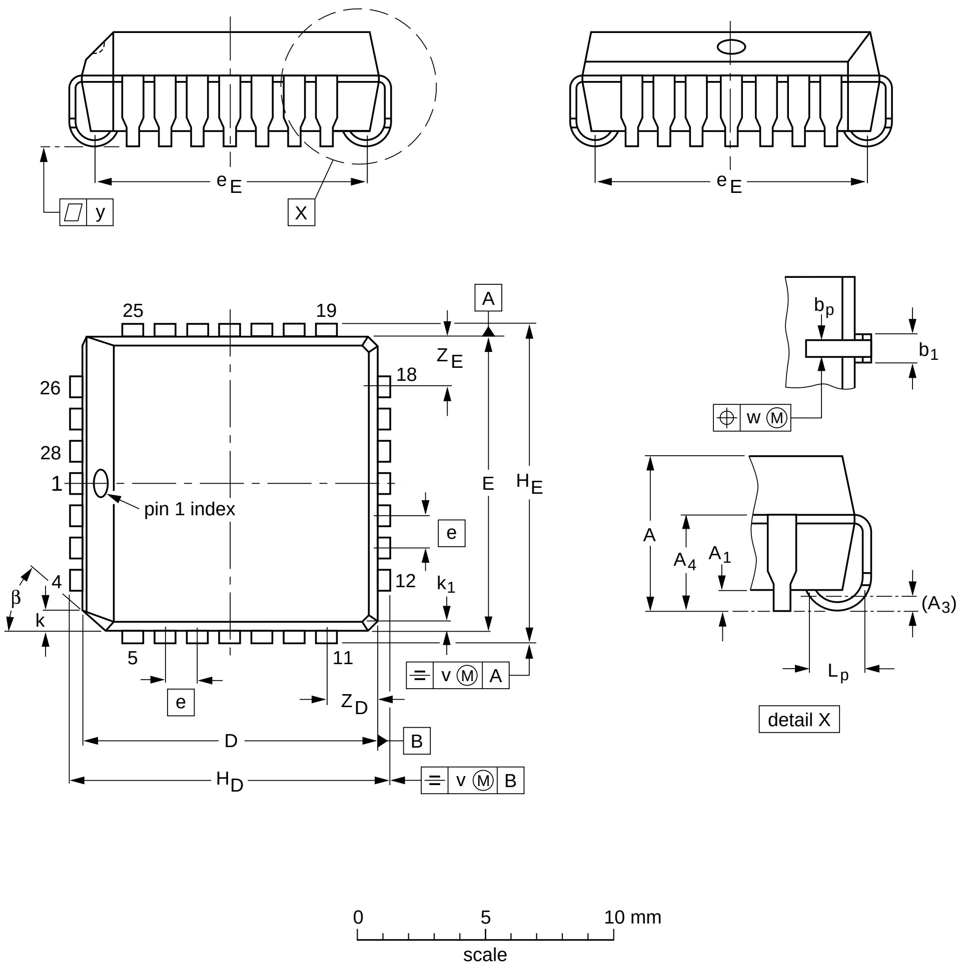
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

PLCC28: plastic leaded chip carrier; 28 leads **SOT261-2**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	A_1 min.	A_3	A_4 max.	b_p	b_1	$D^{(1)}$	$E^{(1)}$	e	e_D	e_E	H_D	H_E	k	k_1 max.	L_p	v	w	y	$Z_D^{(1)}$ max.	$Z_E^{(1)}$ max.	β
mm	4.57 4.19	0.51	0.25	3.05	0.53 0.33	0.81 0.66	11.58 11.43	11.58 11.43	1.27	10.92 9.91	10.92 9.91	12.57 12.32	12.57 12.32	1.22 1.07	0.51	1.44 1.02	0.18	0.18	0.10	2.16	2.16	45^o
inches	0.180 0.165	0.020	0.01	0.12	0.021 0.013	0.032 0.026	0.456 0.450	0.456 0.450	0.05	0.430 0.390	0.430 0.390	0.495 0.485	0.495 0.485	0.048 0.042	0.020	0.057 0.040	0.007	0.007	0.004	0.085	0.085	

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT261-2						~~92-11-17~~ 95-02-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.